ABSTRACT

A compliant semiconductor chip package with fan-in leads and a method for manufacturing the same. The package, or "assembly", contains a multiplicity of bond ribbons connected between the contacts of a semiconductor chip and corresponding terminals on a top surface of a compliant layer. The compliant layer provides stress relief to the bond ribbons encountered during handling or affixing the assembly to an external substrate. The chip package also contains a dielectric layer adjacent to at least one end of the bond ribbons. The dielectric layer relieves mechanical stresses associated with the thermal mismatch of assembly and substrate materials during thermal cycling. The assembly can be manufactured without the need for any bond wiring tools since the bond ribbons are patterned and formed during a standard photolithographic stage within the manufacturing process. The manufacturing process is also amenable to simultaneous assembly of a multiplicity of undiced chips on a wafer or simultaneous assembly of diced chips in a processing boat.

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